What is Claimed:

1. A method for manufacturing an integrated circuit comprising:

(a) forming an opening in a layer for a dual damascene structure; and

(b) forming at least two openings in the layer for a capacitor.

2. The method of claim 1 wherein steps (a) and (b) occur at substantially the same time.

3. The method of claim 1 wherein step (a) further comprises:

(a1) forming a groove; and

(a2) forming a via.

4. The method of claim 3 wherein steps (a1) and (b) occur at substantially the same time.

5. The method of claim 3 wherein steps (a2) and (b) occur at substantially the same time.

6. The method of claim 1 further comprising:

(c) filling the opening with a conductive material to form a dual damascene structure; and

(d) filling the at least two openings with the conductive material to form the capacitor.

7. The method of claim 6 wherein steps (c) and (d) occur at substantially the same time.

8. The method of claim 1 wherein the layer comprises a plurality of layers.

9. The method of claim 8 wherein the plurality of layers includes at least one etch stop layer.

10. A method of manufacturing an integrated circuit comprising:

(a) forming a plurality of layers;

(b) partially forming a dual damascene structure by forming a first opening in at least one of the plurality of layers; and

(c) partially forming a capacitor by forming second and third openings in at least one of the plurality of layers.

11. The method of claim 10 wherein the first, second, and third openings have substantially the same width.

12. The method of claim 10 wherein the second and third openings have a first width and the first opening has a second width different from the first width.

13. An integrated circuit comprising:

a layer;

a dual damascene structure formed in the layer;

a capacitor formed in the layer, the capacitor having a first conductor and a second conductor formed in the layer.

14. The integrated circuit of claim 13 wherein the layer includes at least two layers.

15. The integrated circuit of claim 13 wherein the first conductor and the second conductor are not formed above or below each other.

16. The integrated circuit of claim 13 wherein:

the layer includes a stop layer; and

the dual damascene structure includes at least a groove and a via where a bottom portion of the groove includes at least a top portion of the stop layer.

17. The integrated circuit of claim 16 wherein the stop layer is formed between the first conductor and the second conductor.

18. The integrated circuit of claim 13 wherein the layer includes a stop layer and the stop layer is formed between the first conductor and the second conductor.

19. The integrated circuit of claim 18 wherein the first conductor and the second conductor contact the stop layer.

20. The integrated circuit of claim 19 wherein the first conductor includes a liner and a conductive material.

21. The integrated circuit of claim 13 wherein the first conductor is a first plate of the capacitor and the second conductor forms the second plate of the capacitor.

22. The integrated circuit of claim 13 further comprising a substrate where the layer is formed on the substrate and the layer is at least not formed between the first conductor and the substrate.